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| 09/746,515 | 12/22/2000 | John Baggs | 81862P187 | 1054 |
| Jeffrey S. Smith BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP Seventh Floor 12400 Wilshire Boulevard Los Angeles, CA 90025-1026 | | | EXAMINER | |
| | | | ELALLAM, AHMED | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

| | | Application No. | Applicant(s) | | | |
|---|---|-----------------|-----------------------------|--|--|--|
| Office Action Summary | | 09/746,515 | BAGGS ET AL. | | | |
| | | Examiner | Art Unit | | | |
| | | AHMED ELALLAM | 2662 | | | |
| The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply | | | | | | |
| A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). | | | | | | |
| Status | | | | | | |
| 2a)⊠ 3)□ | Responsive to communication(s) filed on <u>23 December 2004</u> . This action is FINAL . 2b) This action is non-final. Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. | | | | | |
| Disposition of Claims | | | | | | |
| 4)⊠ 5)□ 6)⊠ 7)□ | 4) Claim(s) 1-27 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) is/are allowed. 6) Claim(s) 1-27 is/are rejected. | | | | | |
| Application | on Papers | | | | | |
| 9) The specification is objected to by the Examiner. 10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. | | | | | | |
| Priority u | nder 35 U.S.C. § 119 | | | | | |
| 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. | | | | | | |
| | (s) of References Cited (PTO-892) of Draftsperson's Patent Drawing Review (PTO-948) | 4) | | | | |
| 3) 🛛 Inform | nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) No(s)/Mail Date 12/23/04. | | atent Application (PTO-152) | | | |

DETAILED ACTION

Specification

- The disclosure is objected to because of the following informalities:
 On page 6, lines 10 and 11, the numeral character 250 should be changed to
 "260". Appropriate correction is required.
- 2. Claim 22 is objected to because of the following informalities:

In claim 22, the phrase "a plurality of the digital signal processor" need correction, the term "plurality" refers to plurality of DSP while "the digital signal processor" is in the singular form. Appropriate correction is required.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 7, 19, 20, 21, 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Dorsey et al. (USPN 6,198,751), hereafter referred to as Dorsey.

Referring to claims 1, 7 and 19, Dorsey discloses an apparatus/ method for determining whether a digital signal processor needs a service program stored in an overlay memory (when a packet arrives at a packet translator, it is determined what set of instructions a controller (controller is interpreted as interface manager as in claim 19) needs from an opcode memory in order to provide the particular protocol service (see column 4 line 45 through column 5 line 2 1 and column 7 line 64 through column 8 line

37 and figure 5)) and delivering the service program to the digital signal processor from the overlay memory over a host port interface bus (the appropriate opcode instructions form the opcode memory are sent to the controller over a bus (see column 4 line 45 through column 5 line 21 and column 7 line 64 through column 8 line 37 and item 16 in figure 5)).

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Regarding claim 20, Dorsey discloses that the opcode memory stores various instructions required for all the translations that the Multi-protocol translator MPT (packet translator) is capable of performing. See column 8, lines 2-7. (Claimed overlay memory store a plurality of algorithms). (Examiner, in accordance with the description given to the service program as a software algorithm, the opcode instructions reads on claimed algorithms, because they are software codes that perform specific function).

Regarding claim 21, the apparatus of Dorsey comprises the controller. (Claimed the apparatus further comprising the digital signal processor).

Regarding claim 26, Dorsey discloses that the opcode memory stores various instructions required for all the translations that the Multi-protocol translator MPT (packet translator) is capable of performing. See column 8, lines 2-7. (Examiner interpreted the different set of instructions codes necessary for each different packet protocol translation stored by the opcode memory as being the claimed overlay memory stores the service program and a plurality of other service programs, and the determination of the set of instructions upon packet arrival by the packet translator (as indicated above with reference to claim 1) as being the claimed determining which of

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the service program and the plurality of other service programs are needed by the digital signal processor).

Regarding claim 27, Dorsey discloses the retrieval of opcode instruction by the MPT for processing received packets as being the claimed service program comprises an algorithm and wherein delivering comprises downloading the algorithm to the digital signal processor).

Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey.

Referring to claim 13, Dorsey discloses determining whether a digital signal processor needs a service program stored in an overlay memory (when a packet arrives at a packet translator, it is determined what set of instructions a controller needs from an opcode memory in order to provide the particular protocol service (see column 4 line 45 through column 5 line 21 and column 7 line 64 through column 8 line 37 and figure 5)) and delivering the service program to the digital signal processor from the overlay memory over a host port interface bus (the appropriate opcode instructions form the opcode memory are sent to the controller over a bus (see column 4 line 45 through

column 5 line 21 and column 7 line 64 through column 8 line 37 and item 16 in figure 5)). Dorsey does not disclose that the method is implemented using a computer readable medium. However, it would have been obvious to one skilled in the art at the time of the invention to implement the Dorsey system in this manner because the developmental costs of a software implementation are less than that of a hardware based implementation. Furthermore, software is easier to upgrade than hardware.

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6. Claims 2-6, 8-12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey in view of Pickett (USPN 6,181,694), hereafter referred to as Pickett.

Referring to claims 2-4, 8-10 and 14-16, Dorsey does not disclose generating a data packet from a pulse code modulated data stream using the service program. receiving the pulse code modulation data stream from a public switched telephone network or transmitting the data packet over an internet protocol network. However, Pickett discloses a system wherein POTS data (i.e. PCM data from the PSTN central office) is converted into a packet format and transmitted over a WAN such as the Internet (see figure 3). It would have been obvious to one skilled in the art at the time of the invention to implement this feature into Pickett because communicating PCM data from the PSTN and Internet communications are both very commonly used communications protocols. Therefore, converting between these communications in the Dorsey system would make the system more versatile and flexible in supporting different formats for its users.

Referring to claims 5, 11 and 17, Dorsey does not disclose data packet includes data comprising at least one of voice communication, fax communication, modem communication, video communication, and audio communication. However, Pickett discloses a multi-protocol system that provides fax and voice communication services (see figure 3). It would have been obvious to one skilled in the art at the time of the invention to implement the Dorsey system with this feature because doing so would allow the system to support a variety of communication needs, thereby making the system more flexible and versatile.

Referring to claims 6, 12 and 18, Dorsey does not disclose receiving a packet from an internet protocol network, generating a pulse code modulation data stream from the packet using the service program and transmitting the pulse code modulation data stream over a public switched telephone network. However, Pickett discloses that packet data from the Internet is converted into POTS data (i.e. PCM data for the PSTN) (see figure 3). It would have been obvious to one skilled in the art at the time of the invention to implement this feature into Pickett because Internet communications and communicating PCM data to the PSTN are very commonly used communications protocols. Therefore, converting between these communications in the Dorsey system would make the system more versatile and flexible in supporting different formats for its users.

7. Claim 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey in view of Brown et al USPN 6,747,995), hereinafter referred to as Brown.

Regarding claim 22, Dorsey discloses substantially all the limitation of claim 19 as indicated above with reference to claim 19, except it does not specify that a plurality of digital signal processor coupled to the bus.

However, Brown with reference to figure 5, discloses a plurality of DSP connected to a host port interface bus, see column 10, lines 32-39. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made to modify the architecture of the system of Dorsey to include a plurality of DSP in connection with a an HPI bus as taught by Brown so to increase the throughput of Dorsey system. A person of skill in the art would do so by recognizing the scalability feature of implementing a plurality of DSPs, as well as to the inter-processing capability of the HPI bus standard architecture. It would be also advantageous to single out the malfunctioning of a DSP in case of malfunctioning without impacting the overall operational state of Dorsey system.

Regarding claim 23, in addition to the limitation discloses above with reference to claim 22, Brown also discloses a processor 502 (figure 5) (claimed host port interface manager) coupled to the HPI bus 503, see column 10, lines 32-39. (The processor 502 in combination with the reads on the claimed the interface manager and the host port interface manager, since it provided the same function of the claimed packet pump).

Regarding claim 24, Dorsey in view of Brown discloses substantially all the limitations of claim 23 as indicated above, in addition Brown discloses a PSTN network coupled to transmit a pulse code modulation data stream See column 6, lines 34-49. (Examiner interpreted the transmission of the PCM of Brown as equivalent to the

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claimed transmission of PCM data streams to the packet pump, because there is not further limitation in the claim that further limits the claim limitation other than the transmission).

Regarding claim 25, Dorsey discloses the opcode memory but doesn't specify that the memory is SRAM. However, Brown discloses the use of SRAM by DSPs for program codes and data storage. See column 8, lines 12-13. It would have been obvious to a person of ordinary skill in the art, at the time the invention was made to make the opcode memory of Dorsey being an SRAM memory as taught by Brown so that faster access can be provided in downloading the requested instruction codes by the DSPs. A person of skill in the art would do so by recognizing the advantage the SRAM provides over other types of memories of being faster as well as the reduction in the manufacturing cost by purchasing SRAMs that are widely available in the market.

Response to Arguments

8. Applicant's arguments filed 12/23/2004 have been fully considered but they are not persuasive:

Applicants argue that Dorsey does not disclose the limitations of claim 1, especially Dorsey doesn't disclose a DSP, because the controller of Dorsey is not a DSP, Applicant further stated that DSP is a heterogeneous architecture from that of an ASIC, PLD or general purpose CPU. Examiner respectfully disagrees, the controller of Dorsey, as admitted by Applicants on page 9, third paragraph, may be an ASCI, PLD or a general CPU. Dorsey stated in the brief summary that:

The second approach is to design a custom hardware machine to perform the translation. For this solution, a state machine is hard coded to perform each translation from one format to the other. In the event that the translator 12 must translate from multiple formats to multiple formats, a fast hard coded translator must be designed and implemented for each translation. While common parts of similar translations may be combined to decrease circuitry, this adds significantly to the complexity of hardware verification. The hard coded state machine is usually implemented on an application specific integrated circuit (ASIC) or using a programmable logic device (PLD, such as field programmable gate arrays or complex programmable logic devices).

It follows that from the above description that Dorsey description is related to prior art system and not to the controller. In addition the function provided by the controller of Dorsey reads on that of the claimed DSP. Moreover, DSP are well known in the art, as shown by Brown reference (indicated above).

Applicants also argue that the bus of claim 1 is not similar to the Dorsey's bus, because Dorsey bus is not a host port interface bus. Examiner respectfully disagrees, the claimed "host port interface bus" is simply interpreted as "bus" since it doesn't provide any different functionality other than that provided by Dorsey's bus. Examiner submit that that HPI buses are well established in the art, and they are used for interprocessors communications (inter-DSPs communications), However claim 1 recite one single DSP in connection to the (HPI) bus, it is within this context of a single DSP and a bus that Examiner interpreted the claim limitations.

Examiner believes, given the broadest reasonable interpretation of the claim limitations, the rejection above is proper.

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Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Dick et al, US 2002/0080782), and Reimer et al, US 2002/0059393.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AHMED ELALLAM whose telephone number is (571) 272-3097. The examiner can normally be reached on 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kizou Hassan can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AHMED ELALLAM Examiner Art Unit 2662 May 27, 2005

> HASSAN KIZUU SUPERVISORY PATENT EXAMINER

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